MTech VLSI & ES Dissertation Abstracts 2020-21

VLSI Design for scalable video codec in band motion

Pranav Adhari
(MIS No. : 121935001)

Name of the Guide: Dr. P. P. Shingare

Abstract

Video contain large amount of information that requires large storage, large bandwidths for transmission from encoder to decoder and longer transmission time, so image coding is required to be not only efficient but also scalable. Recent wavelet techniques provide a way for efficient and scalable image coding. The Discrete Wavelet Transform (DWT) is a powerful signal processing tool that has recently gained widespread acceptance in the field of digital image processing. The DWT is useful in the field of image compression where it replaces the conventional Discrete Cosine Tranform (DCT). The design and implementation of a flexible hardware architecture for the 2-D DWT is presented in this thesis. The Lifting Scheme method is used to perform the DWT instead of the less efficient convolutional based methods. Its combined with SPIHT (set partitioning in hierarchical trees) algorithm which is used for compression by finding redundancy among wavelet coefficients. SPIHT has exceptional characteristics over several properties like good image quality, fast coding and decoding, a fully progressive bit stream etc. Furthermore run length encoder is used for more data compression.

Day ahead Estimation of Solar PV plant using ML algorithms

Praveen Aher
(MIS No. : 121935002)

Name of the Guide: Mr. Ranjit Sadakale

Abstract

Solar energy is a key renewable energy source. However, its intermittent nature and potential for use in distributed systems make power prediction an important aspect of grid integration. It is one of the most promising environmental-friendly energy sources. Its market share is increasing rapidly due to advances in Photovoltaic (PV) technologies, which have led to the development of more efficient photovoltaic (PV) solar panels and the significant reduction of their cost.

However, the generated solar energy is influenced by meteorological factors such as solar radiation, cloud cover, rainfall, and temperature. This variability affects negatively the large-scale integration of solar energy into the electricity grid. Accurate forecasting of the power generated by photovoltaic (PV) systems is therefore needed for the successful integration of solar power into the electricity grid. The objective of this project is to explore the possibility of power generation prediction using machine learning methods to accurately predict the generated solar power so that this sustainable energy source can be better utilized.

Real Time Fruit Detection and Recognition for Smart Refrigerator

Avinash Andhale
(MIS No. : 121935003)

Name of the Guide: Dr. P P Bartakke

Abstract

Smart Home Appliances are emerging with new features and technology day by day. One of the essential and common home appliances is Refrigerator which helps to preserve Food and Vegetables. There has been lots of research going to make refrigerator Smart enough to take action. With integrated Camera, Wi-Fi, IOT and Embedded Technology various Smart Refrigerators are available in market. To detect the objects, present inside refrigerator is the current area of research for smart refrigerator. Currently Deep Learning technologies are being applied to detect the objects present in refrigerator. It is necessary to detect the items presents in refrigerator effectively and accurately. Therefore, the focus of the project was to find a low-cost solution to detect the fruits inside the refrigerator more effectively and accurately, so that the user can know the type of fruit, quantity of fruit and quality of fruit from remote place. Inventory has been made available to user on internet. Various algorithm was applied such as Faster-RCNN, SSD, Yolo-V3 and tiny Yolo-V3 for object detection and it is concluded that SSD outperform all other models. comparison has been made based on Speed of detection, Accuracy on real time image, and the compatibility of Hardware. The real time implementation result showed that SSD is best for fruit detection inside refrigerator.

3-phase inverter & PMSM motor plant modeling for HIL controller software testing

Malhar Ashtapure
(MIS No. : 121935004)

Name of the Guide: Prof. M S Sutaone

Abstract

All automotive industries follow V-model for product development. V-model is a graphical representation of system development lifecycle, i.e. process defined for development of a product. See figure 1.1. The V-model has a specific section on testing of the project. The project work highlighted in this thesis addresses testing of traction in electric vehicle. The project work done covers Hardware-in-Loop testing of traction motor control. The work done in this project work may help developers in development of traction motor control algorithm and will reduce development time. The development and testing of traction motor control algorithm is difficult and time consuming. The main goal of the project is to make development and testing of traction motor control algorithm easy for developers. The goal is to reduce development time of traction motor control algorithm. To achieve this goal, project is focused on prototyping of an onbench test solution for traction motor control algorithm. This will help in developing the algorithm without connecting an actual traction motor to motor controller. One of the motives is also to make the solution low cost.

Automatic License Plate Recognition System

Ninad Awalgaonkar
(MIS No. : 121935005)

Name of the Guide: Dr. P P Bartakke

Abstract

Automatic License Plate Recognition system (ALPR) demonstrates an implementation of a deep learning-based approach to locate license plates of four-wheeler vehicles thereby enabling optical character recognition (OCR) to recognize the characters and numbers on the located plates in real-time. ALPR is an image processing technology built on the base of Single Shot Detector architecture. The system works in a three-stage pipeline: Image acquisition, License Plate Detection, and OCR. The webcam with the precise resolution is employed as an image acquisition source. Single Shot Detector (SSD) based MobileNet version 1 model is utilized as a detector. Two Optical Character Recognition (OCR) methods have been employed in this system namely Tesseract OCR and Easy OCR. The system is implemented and tested on two hardware platforms viz. Raspberry Pi 3B and NVIDIA's Jetson Nano. Over a decade number of four-wheeler vehicles in the country has increased tremendously. The overcrowding of vehicles results in traffic congestion, Accidents, and Security concerns. The ALPR is a solution to these problems. This system can be used by the traffic department to identify and penalize rule violators. This system can be employed on borders of the country to detect unauthorized vehicles crossing the border. The ALPR system based on SSD architecture gives a detection accuracy of 95%. The recognition accuracy of the proposed system is 90% for Easy OCR and 62% for Tesseract OCR.

Implementation of Special Load and Store Instruction for the RST Unit

Saurabh Bhosale
(MIS No. : 121935007)

Name of the Guide: Dr. Vanita Agarwal

Abstract

The Rough Set Theory (RST) concept has shown the capability in fields of knowledge extraction, data mining, decision making, pattern recognition, image processing, etc. Along with this RST comes in very handy to draw a conclusion on the incomplete and inconsistent data sets and their effect on the desired output. So having dedicated hardware on RST can be useful for next-generation IoT devices. Such RST based hardware performance may be increased if the ISA has capable of doing Memory Access instruction that can transfer data present at multiple locations at one go. The thesis present the work done on the RTL implementation of datapath and control-path inside ISA to perform Load and Store operations considering multiple locations. This will save the clock cycles taken into consideration to perform data transfers.

Acceleration of Convolution Neural Network using FPGA

Jyoti Doifode
(MIS No. : 121935008)

Name of the Guide: Mr. Ranjeet Sadakale

Abstract

Lately, Deep Learning has indicated its capacity by adequately tackling complex learning issues which were not possible previously. Specifically, Convolutional Neural Networks are most generally utilized and have indicated their viability in image detection and recognition problems. Convolutional Neural Networks (CNN) can be used to perform different kinds of tasks. However, to recognize even a single image, billions of calculations are required. For example, ResNet 50 takes 8 billion calculations just to figure out what's in a single image. So we need to find out ways to be able to run that superfast and that's why we need hardware accelerators. This thesis presents the basic information about Convolutional Neural Networks along with the key operations involved and the brief idea about Field Programmable Gate Arrays(FPGA) is given which enable them to be used for accelerating the inference process of Convolutional Neural Networks. Various techniques which were employed previously for accelerating the Convolutional Neural Networks are discussed. We are focussing on designing a energy efficient Field Programmable Gate Arrays accelerator for accelerating the inference process of Convolutional Neural Networks with reduced latency and increased throughput.

Development of AMBA ACE protocol UVC

Paresh Dukare
(MIS No. : 121935009)

Name of the Guide: Dr. Vaishali Ingale

Abstract

Smart Cartridge Based Washing Machine By Implementing Near Field Communication (NFC)

Aditi Ghongade
(MIS No. : 121935010)

Name of the Guide: Prof. M S Sutaone

Abstract

The Washing machine has a separate container to hold detergent , bleach or fabric softner called Cartridge. This Cartridge is used to dispense the precise amount of detergent at the time of wash cycle. The main ACU (Appliance Control Unit) in washing machine takes care of how much quantity of detergent to be dispensed according to the load .There is a requirement that we should continuously keep track of insertion and removal of cartridge and get the data of how much quantity of detergent was present before dispensing and how much is remained after wash cycle. Also other information like concentration , density and flow rate of liquid detergent. So to meet this objective ,this project implements the wireless mechanism that will accurately track the cartridge and send the detergent related information to ACU for further action. There are various wireless communication technologies available in market such as NFC, Bluetooth , BLE (Bluetooth low energy), RFID, ZigBee, Z wave. Considering the low power and small distance (< 8cm) requirements for this application ,this project aims to establish wireless communication between cartridge and ACU or HMI using NFC (Near Field Communication)technology.

Generic End of Line Testing Platform

Sarang Gokhe
(MIS No. : 121935012)

Name of the Guide: Dr. Vanita agarwal

Abstract

The "End of Line Testing" term is mostly used in the manufacturing industry and is the responsibility of that "End of line Testing Platform" to check for overall operation and functionality of the product/products during the manufacturing process or after calibration of the product or before delivered it to the customer or end-user. Under any harsh conditions in the manufacturing environment, the testing system must simulate all appropriate conditions, whilst reproducing the same measuring the responses of equipment being tested. In series of production, a high testing output rate is important. For the same reason, the testing procedure was developed to optimize in order to achieve a short cycle time of testing. This EOL testing is also helpful to meet the quality control parameter of that particular product and to ensure not a faulty product to be delivered to the customer side. The main advantages of such EOL testing platforms are reducing EOL test cost, increasing production throughput, it helps by identification of faults and errors in design and can be useful for improvement of design. It helps in the reduction of manpower needed for manual testing. Generic EOL testing platform is also useful for testing other products with low complexity and helps to improve the cycle time required for each testing.

Reconfigurable Cache Memory Model with AMBA ACE interface

Kshitij Gurjar

(MIS No. : 121935013)

Name of the Guide: Dr. Vaishali Ingle

Abstract

In current semiconductor environment, high performance, high speed processing power of a processor is a major point of focus. In order to achieve it, the required data which is to be processed must have minimal latency to fetch from memory. To enable it, Cache memories are developed which resides adjacent to the processor die. This enables faster data and instruction fetch for the processor. But the data exchange between processor and different cache must also follow a coherency model as today's processors are multi-cores. AMBA ACE protocol is such a protocol which is swiftly allowing the coherency to take place among multi-cores. During development of such cache based systems, it becomes essential to verify them functionally by putting them in a regressive verification environment. Such an environment needs a Cache Memory Model which will support data to maintain coherency for interconnects. This Cache Model supports the ACE protocol and ACE signals which can be deployed with the ACE interface. It is a Reconfigurable Cache memory model which supports all the 16 transactions defined by ACE protocol and processes the data based on the availability in cache in terms of cache hits or miss and replaces a fully occupied cache set according to the cache replacement policy of Least Recently Used (LRU).

Complexity Reduction of HEVC at Intra- Prediction Level

Poojal Jadhav
(MIS No. : 121935014)

Name of the Guide: Mrs. Yogita Vaidya

Abstract

The High Efficiency Video Coding (HEVC) has been designed with the perspective to drastically reduce bit rate with no compromise with the video quality. The key feature that differentiates H.265 from H.264 include increased number of modes from 9 to 35, and the introduction of larger block structures with flexible block sizes from 64 x 64 to 8 x 8 samples. It is evident that the enhanced feature has imposed higher complexity specifically at the intra prediction level of HEVC. The proposed paper presents detailed analysis of complexity at intra prediction level of HEVC. We further explore the different machine learning approaches suitable to address the complexity issue at Intra prediction and present a novel machine learning approach to simplify the intra mode selection and early terminate the Coding Unit partitioning. The proposed method achieves two-fold performance improvements in terms of complexity reduction, since the overhead of modes for Rate Distortion RDO process is decreased the encoding time is reduced by average of about 35 % when compared with HM16.15 reference model. The approach is novel in the sense that we employed RBF kernel which accounts for the slight non linearity between the class label and attributes. It is observed that the proposed approach increases the classification accuracy by 5 % when compared with other approaches in the literature. The encoding complexity of intra prediction mode in HEVC is reduced with ETH-CNN to determine the partition of the CU instead of using the brute-force search. Finally, experimental results show that with reduction in complexity, we have achieved good accuracy of intra prediction mode in HEVC.

Audio Processing for Tones Validation using Deep Learning

Padmini Pandhare
(MIS No. : 121935015)

Name of the Guide: Dr. Vaishali Ingle

Abstract

Audio signal validation of products presents special problems in Industry. Automation is a key to throughput, but any analog system is hard to analyze. Audio signal validation is a tricky and time-consuming part. This work presents automation of audio tones validation which confirms audio content and quality. In this thesis , we propose an audio classification method based on Convolutional Neural Network technique, which originated from a deep learning field and extract features from the spectrogram. The proposed method processes signals, analyzes the model, classifies, and predicts the audio signal. The selected algorithm identifies all the tones from different categories which are recorded by the microphone. Microwave tones are taken as a

case study and evaluate a proposed approach. This approach thus provides a feasible solution for different categories of products. The experimental results clarify the effectiveness of the proposed method to achieve higher accuracy of audio tone validation.

Neuromorphic computing: Modelling of 3D integrated circuit components using TSV

Vaibhav Takawadekar
(MIS No. : 121935018)

Name of the Guide: Mrs. Y M Vaidya

Abstract

Over the years transistor size is reduced such that now we are on the edge of Moore's law. To overcome this problem and to feed the need of better processors, multi-chip packaging (3D) technologies have evolved as well as new approach of computer architectures, complimentary to existing one, have developed. A major component of 3D IC is Through Silicon Via. Through-silicon vias (TSVs) directly connects die-to-die stacked structures. In the process parasitic of the IC is also changed. In this work, a TSV structure is generated and analyzed in HFSS with a view to understand its parasitics. And the same is compared to interconnects used in equivalent 2D IC. ITRS road-map provides standardization in silicon dimensions. Following these standards, a model of TSV is generated and simulated in HFSS to analyze, measure impact of TSV on capacitance, inductance, resistance as well as cross-talk. High density, effectively packed silicon devices can be manufactured using TSV technique. In Neuromorphic computing (NC), processing and storing of data is done at the same place. NC plays key role in making faster processors for next generations of computers as well as in making of dedicated hardware for ML, AI applications. This work also mentions possibilities of use of TSV to create dedicated Neuromorphic components and its effect.

Automated Optical Inspection Using Computer Vision and Deep Learning

Ayushi Tapar
(MIS No. : 121935019)

Name of the Guide: Dr. P P Bartakke

Abstract

Automated Optical Inspection (AOI) is one of the fastest growing use-case of AI/ML techniques and has plethora of applications in manufacturing plants and industries. Major advantage of AOI is human-free monitoring of production line to detect faults. The project work highlighted in this report demonstrates two problems statements which are addressed using AOI: 1. Weak

Supervised Learning (WSL) on INTEMO-Firewall dataset and 2. INTEMO GAPv2 detection. In INTEMO Firewall project, the task is to classify the magnetic rivets that fit onto a control panel into defective and non-defective rivets. Main challenge in this project is: the dataset contains huge amount of unlabeled data. Various techniques for labeling unlabeled data are highlighted, focusing on Weak Supervision technique which generates weak labels for unlabeled data using various weak supervision sources. A Weak Supervised Learning pipeline is implemented to obtain weak labels for unlabeled data. Finally, a master (Convolutional Neural Network) CNN model is trained with labels obtained with WSL pipeline and the results are compared with the model trained only with labeled data. INTEMO Gapv2 detection project involves detection of gap width between two plates in the internal structure of a headlamp actuator in production line. The gap width within a certain range is mandatory for correct functioning of the actuator. CV-based classifiers are implemented to detect the gap and measure the gap width in pixels and an attempt is made to improve the false negatives rate of the existing classifier which is currently deployed in production. AOI techniques are largely useful to segregate defective pieces in a production line, thus resulting in huge cost savings and reduced human labour.

***