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Implementation of rule based testing for digital circuits using inductive logic programming

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Abstract

Inductive logic is widely known for implementing a rule based system. This rule mainly represents basic logic for digital circuits. In this project we are implementing optimized inductive logic i.e Metarule. This metarule is optimized from inductive logic programming. The main aim of the thesis is to simplify the digital testing process with the help of metarule. Using metarule we can implement the circuit logic with some simple code. This code based designs make a quick and simple solution for digital circuit testing.

Design of Similarity Detector using Hashing on FPGA

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Abstract

For the purpose of Similarity detection many reaches implemented the similarity detection algorithm (Bloom Filter, Hamming Distance, Levenshtein Distance) on software as well as on hardware, this will alone work efficiently but cannot be useful when it comes to detect similarity between large files as it compares byte by byte, so to overcome this limitation, Hashing algorithms are used to compress the file, these methods are also known as Fuzzy hashing. There are many projects on Fuzzy hashing which are implemented on software but no one has implemented the fuzzy hashing on Hardware. In this thesis we have used Levenshtein Distance Algorithm (Minimum Edit Distance) as similarity matching algorithm, This thesis presents Segmenting the input file into pseudo random length blocks or segments, Hash value for each segment is computed using modified MD5 hashing algorithm and result is 32 bit hash value called as signature, after collecting all the signatures of an input file, these signatures are compared with the signatures of other input file.

Hardware Implementation of HEVC Intra Prediction Encoder

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Abstract

HEVC (High Efficiency Video Coding) is the successive video coding standard of the established H.264/AVC aiming to reduce bitrate of about 50% while preserving same picture quality. To achieve such a good coding efficiency, several techniques are applied of which each includes different coding tools. Intra-picture prediction is an imperative part of High Efficiency Video Coding (HEVC/H.265) standard, which predicts the spatial correlation within a frame to remove redundancy. The intra-prediction process specified in HEVC/H.265 is computationally intensive and is relatively slow. Therefore, hardware implementation is desirable to accelerate the process. This thesis presents an efficient implementation of intra-prediction in an HEVC coder using Verilog HDL. Each of the 35 modes of intra-prediction are included in the design, viz. DC, planar, and 33 angular prediction modes. Intra-prediction is performed on the Luma as well as Chroma signal of an input image. Quality analysis of the test benchmark is done using distinct criteria, namely visual quality, Peak Signal to Noise Ratio (PSNR).

Development of AXI4 Interconnect UVC using SV (UVM)

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Abstract

Now-a-days to achieve early tape out industries prefer to use proven design IP and integrate them with other IP's to create a system on chip (SoC). In order to make sure all the IP's can communicate with each other we need to use an interconnect fabric that will connect different IP's together. AXI is a communication protocol used for communication between different components inside the SoC. Main advantage of AXI protocol is that all the channel are pipelined and can operate independent of each other. Once the design is complete it needs to be verified by running it through different test scenario. Thus verification is an important process in development of a SoC in VLSI design flow. The verification environment is incomplete without an interconnect component present within. It helps to simulate real-life scenarios as SoC contain multiple IP's interconnected together. Thus for complete verification of a SoC the role of interconnect as a verification component is crucial. The project implements such a verification component which communicates using AXI4 protocol and carries out multiple test scenarios to ensure that the desired results are achieved.

Design of 100mV Low-Dropout Voltage Regulator having Fast Transient Response in 180nm Technology

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Abstract

Power management circuit is an important part of any circuit design. As the technology is scaled down the power supply of the devices also scaled down with the same factor, so it becomes very important to supply a constant voltage to each part of design elements for its faithful operating condition. In this thesis, a single stage linear regulator with an input supply of 2-1.8 V and output voltage of 1.7 V is implemented on 180nm technology. Quiescent current and full load current of LDO is 111.97uA and 20mA. The settling time of LDO is 20us. A high gain folded cascode amplifier of 60db gain and 89deg phase margin has been used as an error amplifier.

Prognosis of BLDC motor using Signal Processing Techniques

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Abstract

Analysis of the demagnetized permanent magnets in BLDC motor is presented in this paper. Automotive, aerospace, consumer, medical and industrial applications are the fastest growing markets for Brushless DC (BLDC) Motor. BLDC motor has high efficiency, high power density, and low maintenance cost. Still, due to overloading the motor, lots of faults can occur in stator, rotor, bearings and permanent magnets. In this paper, focus has been given on faults in permanent magnets. Modeling of demagnetized BLDC motor is presented using MATLAB/SIMULINK and AWT (Analytic Wavelet Transform) analysis is also done to find time frequency ridges. Test results show that stator current peak increases as magnets are demagnetized.

Fruit Detection and Recognition for Smart Refrigerator

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Abstract

Food image recognition is one of the promising applications of visual object recognition in computer vision. Inappropriate diet and too much calorie intake have been key factors causing these health risks and hence keeping a check on the calorie consumption can help to avoid this problem. The intelligent refrigerator is capable of sensing and monitoring its contents and counts the age of the contents. The aim of this project is to analyse the items present in fridge and notify the customer with the updated list of products present. The nutrient content of these items is calculated and presented to the customer. The model was trained to the small amount of the data set and got 78.

Design of Low Power Phase-Locked Loop (PLL) using 90nm CMOS technology

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Abstract

The PLL is a negative feedback control system which having digital as well as analog signal processing units, so it is a mixed signal circuit. The main objective of this work is to optimize pll for low power, low pull in time and low jitter using the 90 nm CMOS technology in the cadence virtuoso tool. As we know voltage-controlled oscillator (VCO) is the crucial block of the PLL which consumes most of the power, so the optimization of the VCO circuit is performed by the convex optimization technique. For this thesis, a current starved voltage controlled oscillator has considered over other oscillators because of its low power consumption, less on chip area, wide bandwidth and don't need to used passive components like inductor and capacitor. The results of designed PLL are power dissipation is 5.4mW from 1 V DC supply and 1GHz output frequency from 500Mhz reference frequency. The lock-in time of PLL is 100ns and 11.08ps clock jitter. The analysis and comparison of results of the CSVCO designed using the convex optimization technique and conventional ring oscillator and LC base oscillator. The results of pull-in time, clock jitter, output frequency, power dissipation are observed and conclude using the simulation tool.

Hand Wash Compliance using Computer Vision Approach

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Abstract

The proper execution of hand hygiene during key moments of patient care is very significant way fro preventing the healthcare associated infection. In hand hygiene improvement many methods are aimed but the compliance rate of hand hygiene is remained minimum. The system which will provide the hand hygiene performed by health care workers (HCWs). Direct observational Hand wash methods have reported the weaknesses in the area. We have reported hand wash compliance using computer vision approach. In computer vision approach we observing the hand hygiene opportunities and disinfection's compliance of HCWs we calculated against the video recording . Using Deep learning algorithm the hand wash steps which are recommended by the world health organization guidelines for hand wash process. This work mainly focused on identifying the hand wash process(HWP) steps correctly. As WHO recommended that hand wash steps motion is important than just checking steps are carried out Using video classification by visual geometry group-16 (VGG-16) and long Short Term Memory (LSTM) architecture. Using VGG-16 architecture feature extraction from the given data set and that extracted features are applied to the LSTM architecture for the further classification. In VGG-16 last softmax layer is removed and directly applied that extracted features as input to the LSTM network. In this method we get the maximum hand wash step validation accuracy in the range of 96%.This method results in good validation accuracy of each step.

Rapid Prototyping of Two Wheeler ABS ECU

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Abstract

With the increasing two-wheeler population, traffic accidents will increase. Surveys and studies about accidents show that it can be reduced by the use of an Anti-lock braking system. The anti-lock braking system is safety-critical and very useful for both driver of two-wheeler and other road users from the safety point of view in emergency braking. The anti-lock braking system reduces the accidents by regulating the wheel slip ratio at optimal value and it is done by monitoring the vehicle speed and wheel speed. In this project, the prototype of an ABS ECU for two-wheeler is developed and it is mainly focused on software development of ECU. The software development involves establish communication between ECU components (Microcontroller and ABS ASIC) and also establish communication between ECU and Tester device for analyzing faults in ECU due to failure of any components or any other reason. The developed software is tested using the Hardware in the loop setup and vector CANalyzer..

Optimization of Memory Oriented Network-on-Chip for FPGA

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Abstract

In this analysis we identify that by the bottleneck link interconnect throughput is limited, tons of files gets created automatically in cache and speed of the network becomes slow down also sometimes system gets hang. Hence we are describing Optimization of cache memory by analyzing the Network on chip (NoC) and field programmable gate array. To address the concerns of conventional bus technology Networks on Chips are proposed as a solution. In this paper with the help of ring topology we are introducing the DWT. To compress the cache memory Discrete Wavelet Transform (DWT) is used. By implementing this proposed method System will get faster. Using the terms of FPGA, we believe that our implementation system will provide high gain and less intricacy.

Semi-Autonomous Park Assist System – Parking Space identification

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Abstract

This project proposes a low-cost Semi-Autonomous park assist system for parallel parking. There are various sensors to identify the parking space, such as an ultrasonic sensor, camera, radar sensor, lidar sensor, and a laser sensor. Park assist systems are already installed in costly cars that use either camera or combination of camera and ultrasonic sensors. To implement a park assist system for average budget vehicles, this proposed system uses only two ultrasonic sensors in front of the vehicle on both sides. To locate the vehicle in the ultrasonic range, an ultrasonic sensors on front side and wheel speed sensor that is installed in cars are used. The value of a wheel speed sensor is received using CAN communication. The hardware architecture contains an ECU module, sensors module, and CAN communication system. The software architecture includes the initialization of the system, hardware diagnostic code, and control algorithm for the system. Various algorithms are already implemented to reduce the error that occurs due to the use of the ultrasonic sensor for edge detection at a curved surface. An algorithm is proposed to minimize the obstacle edge detection. Experimentation was performed before implementing the prototype. The experiment used an ECU board and software used for

calibrating the ultrasonic sensor. The result of this experiment shows that the proposed algorithm has fewer errors compared to previous algorithms. Based on this experiment a prototype for a semi-autonomous park assist system was implemented.

Implementation of Lower and Upper Approximation Features of Rough Set theory on FPGA

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Abstract

Numerous analysts have proposed usage of Rough Set Theory on hard-ware level however not every one of them have built a RTL code for it. Rough set algorithms have been demonstrating their significance in the fields of artificial intelligence, medicine, mining, machine learning, and military purpose and etc. This project mainly focused on writing HDL for the implementation of rough set theory and used this RTL code for obtaining lower and upper approximation features of rough set theory. Having a dedicated hardware for rough set theory can save time and energy. In this project we constructed a RTL for Lower and Upper approximation.

Porting and Optimization of Deep Neural Networks to Embedded Platforms

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Abstract

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Development of Verification IP for AXI-4 Protocol using Universal Verification Methodology

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Abstract

The rising demand of logic circuit that can be fabricated into a single, as small as possible, silicon chip is leading towards the development and designing of more integrated System on Chip (SoC) designs. The increasing need of CMOS technologies has triggered the design of more complex digital systems using reusable Verification IP's. This verification IPs performs the verification of such complex SoC designs in reduced time span and increase the functionality checks of the design. Nowadays, AMBA protocols are highly used standard SoC protocol bus in VLSI industry. These VIPs precisely monitors and detects the functionality errors with easy which makes designing process of complex SoCs easy. The AMBA AXI4 protocol offers high performance, high-frequency and power efficient system designs. AXI4 Protocol is compatible for high-bandwidth, low-latency designs and offers high frequency operation. This protocol is flexible to implement the multiple master-slave interconnect logic, also it is backward compatible with existing APB and AHB interfaces. This project is undertaken to design the Verification IP(VIP) for single master and single slave in SystemVerilog HDL and the burst mode transactions of AMBA AXI4 Master-Slave Interface are verified using Universal Verification Methodology (UVM) and waveforms of signals and simulation results are shown in Mentor Graphics Questasim.

Design and Analysis of Combinational Circuits Using Memristor

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Abstract

So far three essential detached segments have been utilized to structure electronic circuits: resistors, capacitors, and inductors. The fourth essential aloof component is known as the "memristor". That component is known as a memristor in light of the fact that it consolidates the conduct of memory and resistors. The memristor is a two-terminal part whose obstruction relies upon the size and bearing and the span of the applied voltage. The primary memory gadget was presented in 2008 by HP Labs. In the thesis, the LT Spice model portrayed for the memristor is consequently developed as an open model, permitting extra adjustments to be made in extra terms without direct limits. Its usefulness is clarified by applying different window capacities.

SPEECH CONTROL SYSTEM FOR HUMAN-CAR INTERFACE

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Abstract

With the advent of intelligent technologies being integrated inside cars, adjusting and controlling such technologies require driver's attention taken off the road. Driver distraction is one of the causes of the road fatalities happening every year. Improving driver convenience while maintaining a high safety level is one of the hardest challenges of modern car designers. Thus, the speech control system is expected to allow drivers to focus on their essential tasks of driving keeping their eye on the road while driving and help them carrying out the other tasks with ease.
We are supposed to develop a speech control system for the various control interfaces inside car such as infotainment system, air vents on the dashboard, decorative lighting inside the car etc. It will lead to car safety and comfortable drive for the driver as well as passengers.

AUTOMATIC LICENSE PLATE RECOGNITION SYSTEM

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Abstract

Most of India's major cities such as Delhi, Bangalore, Chennai, Hyderabad, Pune, etc. are now home to more than a million vehicles, all of which contribute to traffic congestion & high road accidents. Traffic management in such cities has become a significant issue. Thus there's a desire of an automatic system of traffic police investigation ready to be able to manage the massive traffic on roads with none human intervention. ALPR provides an automatic system to observe and acknowledge the number-plate of cars.
This system will be employed in traffic management system to penalize traffic law offenders, and also be employed in security of parking areas. ALPR consists of 4 stages specifically Image Acquisition, Registration number-plate localization, Character segmentation and Character recognition; registration number plate localization being the foremost necessary one.
This project provides methodology for implementing ALPR using an open source C/C++ library referred to as OpenALPR, supported OpenCV and Tesseract OCR. The elemental goal of the system is to use image processing to detect registration number-plate of the vehicle. The hardware is enforced with Raspberry Pi 3 Model B, and a Pi Noir camera.

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